
CDB47L35-M-1 Layout Guidelines

INTRODUCTION

This document describes the layout Guidelines for the CDB47L35-M-1 customer board. This is intended to be read in conjunction with the schematic and layout files:

- Schematic: CDB47L35-M-1-REV2_SCH.pdf
- Layout: CDB47L35-M-1-REV2_PCB.pdf

GENERAL BOARD CONSIDERATIONS

1. Avoid routing digital signals between power planes on an adjacent layer.
2. The layer stack can be seen in
 - CDB47L35-M-1-REV2_PCB.pdf
3. Avoid routing analogue and digital signals next to each other
 - Particularly important in the audio frequency range, e.g. 8 kHz LRCLK
4. Minimise inductance and resistance between power source and CS47L35 power pins.

LAYOUT GUIDELINES

Analogue Inputs

- Route analogue inputs differentially
- Match impedance of input pairs and track together. **[Medium Priority]**
- Keep inputs away from high speed signals. **[High Priority]**
- Mixed analogue/digital inputs are IN1A and IN2
- Analogue only input is IN1B
- Route analogue input tracks between power/gnd planes if possible

HPOUT

- Route HPOUTL & HPOUTR as a pair. **[Medium Priority]**
- Route MICDET1/HPOUTFB2 & HPOUTFB1/MICDET2 between HPOUT1L and HPOUT1R. **[High Priority]**
- The HPOUT1 signals should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) **[Medium Priority]**

	Min	Typ	Max	Units
DC Resistance		< 0.06		Ω

EPOUT

- Route EPOUTP & EPOUTN as a pair. **[Medium Priority]**
- The EPOUT signals should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.08 Ohms for 8 ohm load) **[Medium Priority]**

	Min	Typ	Max	Units
DC Resistance		< 0.08		Ω

SPKOUT

- Route SPKOUTP & SPKOUTN as a pair. **[Medium Priority]**
- The SPKOUT signals should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.04 Ohms for 4 ohm load) **[Medium Priority]**

	Min	Typ	Max	Units
DC Resistance		< 0.04		Ω

PDM Outputs [Low Priority]

- Route PDM Outputs (SPKCLK and SPKDAT) as a pair.

Device Decoupling [Medium/High Priority]

- Place de-coupling capacitors close to CS47L35.
- Minimise loop inductance between decoupling capacitor and CS47L35 power/ground pins
- Use power planes; short wide traces; multiple vias

External Capacitor Placement Priority

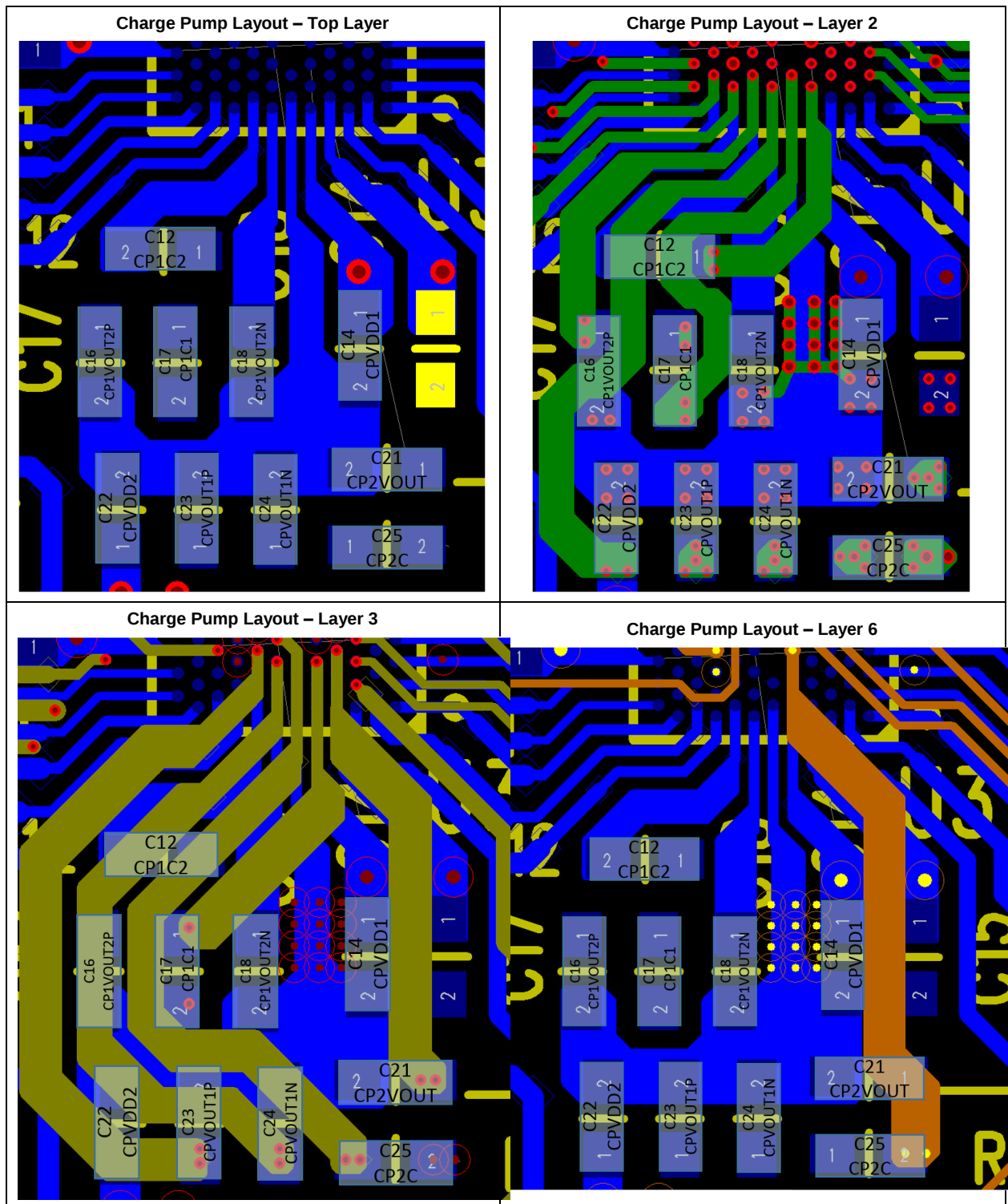
Priority	
1	Vref Cap SPKVDD decoupling DCVDD decoupling
2	CP1C2n flyback CP1VOUT2n CPVDD1 Decoupling CPVDD2 Decoupling AVDD Decoupling FLLVDD Decoupling
2	CP1VOUT1n CP1C1n flyback MICBIAS Output Caps
4	CP2Cn flyback CP2VOUT DBVDD Decoupling MICVDD Output Cap

1V2 Supply [Medium Priority]

- Star DCVDD and CPVDD2 supplies separately to VDDCORE supply
- An RC filter is recommended on FLLVDD, see “Recommended External Components” in the latest datasheet.
- If the DCVDD track is routed through more than 1 layer. There should be 2-4 Via's for each layer transition to reduce the impedance between DCVDD and supply.

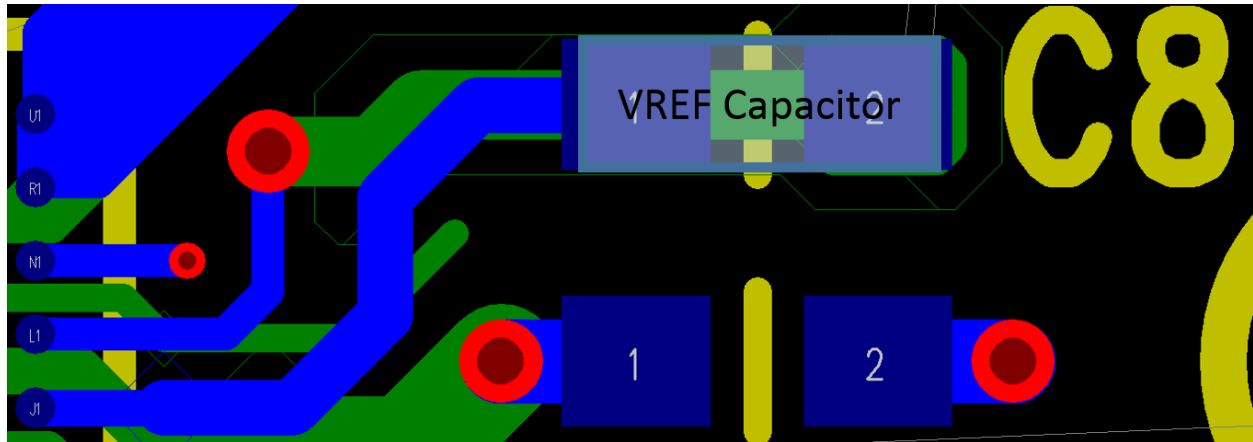
Charge Pumps [High Priority]

- A local ground plane should be used for CPGND and the charge pump de-coupling. The local ground plane should be connected to the common ground plane close to the CPVDD1 and CPVDD2 de-coupling caps (C14, C22).
- VIAs to all GND planes should be placed under the local ground plane. (4 - 8 VIA's)
- Order of priority in relation to charge pump components can be seen in the table above.



VREFC GND Return [High Priority]

The VREFC cap current return path should be routed to AGND1 (Pin L1). AGND should be connected to the GND plane at the pin.

**Digital Signals**

- Use controlled 50Ω characteristic impedance for digital signals. [Low Priority]
- Place series termination resistors close to DUT. [Medium Priority]

Speaker Protection Current Sense Resistors. [High Priority]

- Place R12 close to SPKGNDP (U3)
- Place R13 close to SPKGNDN (R3)

Slimbus Interface [Low Priority]

- Place SLIMCLK R-C network close to DUT. (C1, R6)

Headset Connections [Medium/High Priority]

- For MICDET functionality, MICBIAS2B must not be used for headset connections.
- IN1Bxx inputs should be used for headset connections (due to lower minimum ABSMAX rating.)
- Correct connection of the HPOUTFBn pins (close to the jack socket) will attenuate any noise on the ground plane and reduce crosstalk.

Star connect IN1BLP, MICDET1/HPOUTFB2 and SP5 at J1:P1.

- Use a low impedance connection between J1:P1 and SP5.
- Use a low impedance connection between SP1 and the ground plane.
- Use a low impedance connection between U2:P1 and the ground plane
- Use a low impedance connection between J1:P1 and U2:P6&P8

Star connect IN1BLN, HPOUTFB2/MICDET2 and SP6 at J4:P3.

- Use a low impedance connection between J1:P3 and SP6.
- Use a low impedance connection between SP6 and the ground plane.
- Use a low impedance connection between U2:P4 and the ground plane
- Use a low impedance connection between J1:P3 and U2:P3&P7

KEY TO LAYOUT ITEM PRIORITY

Priority	Description
High	Items of high priority must be followed by the customer. If not, this will affect the correct operation of the Cirrus device.
Medium	Items of Medium priority, if not followed may potentially affect the performance of the Cirrus device.
Low	Items of Low priority are listed as a 'good practice' measure.

SYSTEM ESD GUIDELINES FOR HEADSET

ESD PROTECTION DIODES

The customer should make sure the response time of any ESD protection Diodes used can protect the system for a broad spectrum of ESD transient pulses, from very fast, to extremely slow for large and small ESD voltages.

When testing ESD performance of a system, testing with different contact discharge waveforms from 500V to 8kV in incremental steps, helps verify the selected ESD protection devices can sufficiently protect the system.

BOARD SCHEMATIC OPTIMIZATION

Component placement and board layout are as important as selecting the most suitable ESD protection components. Figure 1 shows a typical combined ESD and EMI circuit protection for a headphone output.

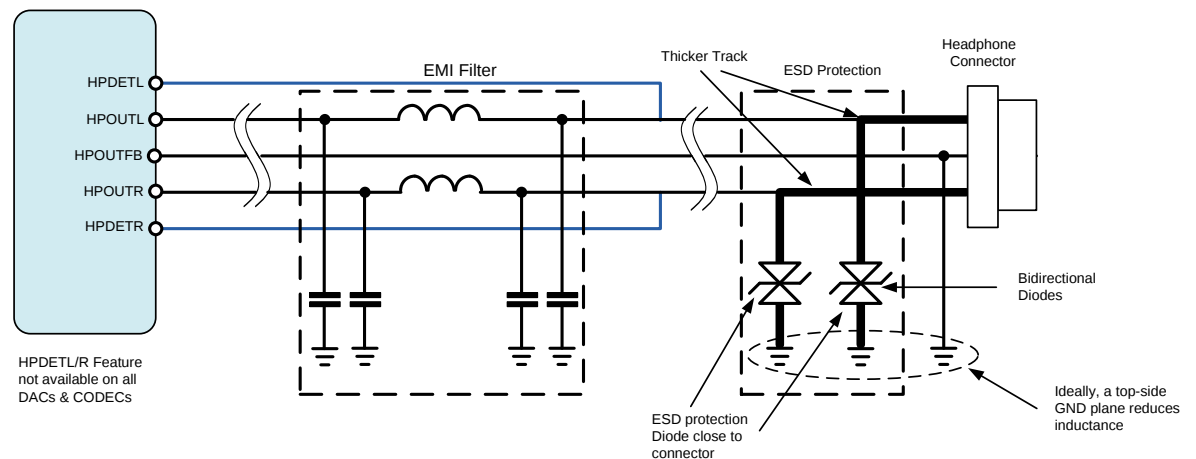


Figure 1 combined ESD and EMI protection

POSITION OF ESD PROTECTION COMPONENTS

PCB layout is critical when using ESD protection components. The ESD protection device should protect the whole PCB, not just the Cirrus Logic device, by diverting the discharge to ground and not letting it pass through the ICs. The following guidelines, as well as any stated on the ESD protection devices manufacturer's datasheet for ESD protection should be followed:

1. The ESD protection device should be placed as close to the connector as possible.
2. The ESD protection device should be placed on the line to be protected, *not* joined by a track stub, which adds inductance
3. The ESD protection device must have a short return path to ground to reduce inductance. A good way to achieve this is to place a pair of GND vias as close as possible to the GND pin of the ESD protection device and the GND pin of the connector, as shown in Figure 2. The double via technique reduces inductance. The best way to achieve it is a GND plane added to the top side of the PCB, to link the ESD diode and connector, as shown in Figure 3. This top side plane must have several vias to the main PCB GND plane in case the discharge path from the connector goes to another part of the end-product.
4. Don't share the GND return path between more than one ESD protection devices, unless it is via a low inductance GND plane.
5. Wide signal tracks from the connector to the protection device reduce the inductance for the ESD charge.
6. Figure 2 and Figure 3 below summaries the above suggestions

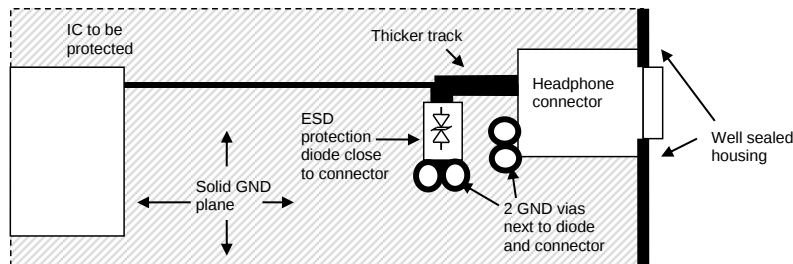


Figure 2 simplistic diagram showing placement of ESD protection diode

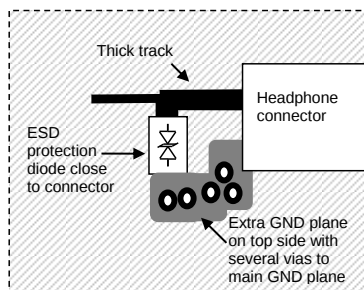


Figure 3 Best practice of top side GND plane between ESD diode and connector

Please consult the datasheet of the ESD protection diode for further advice.

TECHNICAL SUPPORT

If you require more information or require technical support, please contact one of the Cirrus Logic regional offices. To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
01/11/2016	1.0	Original document created		Calum Cuthill

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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